Simple non-galvanic flip-chip integration method for hybrid quantum systems

K. J. Satzinger,[1,2,a)] C. R. Conner,[2] A. Bienfait,[2] H.-S. Chang,[2] Ming-Han Chou,[2,3] A. Y. Cleland,[2] É. Dumur,[2,4] J. Grebel,[2] G. A. Peairs,[1,2] R. G. Povey,[2,3] S. J. Whiteley,[2,3] Y. P. Zhong,[2] D. D. Awschalom,[2,4] D. I. Schuster,[3] and A. N. Cleland[2,4,b)]

[1)] *Department of Physics, University of California, Santa Barbara, California 93106, USA*

[2)] *Institute for Molecular Engineering, University of Chicago, Illinois 60637, USA*

[3)] *Department of Physics, University of Chicago, Illinois 60637, USA*

[4)] *Institute for Molecular Engineering and Materials Science Division, Argonne National Laboratory, Argonne, Illinois 60439, USA*

(Dated: 16 December 2018)

A challenge faced by experimenters interested in exploring hybrid quantum systems is how to integrate and interconnect different materials and different substrates in a quantum-coherent fashion. Here we present a simple and inexpensive flip-chip bonding process, suitable for integrating hybrid quantum devices on chips from different substrates, prepared using separate processes. The process only requires equipment and materials used routinely for contact photolithography, and it is possible to undo the bonding and reuse the separate chips. The technique is relatively gentle, requiring minimal compressive force, and is thus compatible with a wide range of different substrates and materials. Unlike indium-based bonding, this process does not establish a galvanic connection between the two chips, but as we show, in some situations this is not necessary. We demonstrate the technique using lithographically-patterned quarter-wave coplanar waveguide resonators, fabricated on one chip, and couple these inductively to a transmission line patterned lithographically on a separate chip. The two chips have a vertical inter-chip gap of about 7 µm, and we can repeatedly achieve lateral alignments of better than 2 µm. We measure electromagnetic resonances with low-power (~ 1 photon) internal quality factors Q_i around 5×10^5, comparable to single-chip performances, with as-designed coupling quality factors Q_c ranging from 2×10^2 to 5×10^5.

Hybrid quantum systems, comprising multiple interacting quantum devices, represent a flexible approach to solving a range of scientific and practical problems. Such approaches enable, for example, the integration of systems with distinct performance advantages, such as high-fidelity gates in one system combined with long coherence times in another.[1–8] However, it is technically challenging to integrate devices that involve incompatible materials or fabrication processes. One approach, borrowed from the semiconductor industry, is flip-chip integration, where two separate chips are joined face-to-face.[9,10] Recently, efforts to scale up superconducting quantum circuits have involved flip-chip integration with indium bump-bonds, where the indium establishes a superconducting galvanic connection between the two chips.[11,12] While promising, these processes involve multiple metallization steps with challenging surface treatments, require significant compressive force to establish good bonding, and the bonding itself is performed with expensive, specialized equipment.

Here we present an alternative, simple and highly accessible method for flip-chip integration. Instead of making galvanic connections with metal bumps, we bond the substrates using dried photoresist; other materials could be used, but this allows re-use of the chips by releasing in a photoresist solvent such as acetone. The chip-to-chip vertical spacing is established using photolithographically-patterned epoxy spacers. The thickness of the spacers can range from 1 µm to 100 µm, set by the available cured epoxy thicknesses. After manually applying a small amount of photoresist to the periphery of one chip, we place the chips in a standard contact mask aligner, align the chips, and bring them into contact, holding them in place while allowing the photoresist to dry. This involves just one lithographic process beyond what is needed to fabricate the individual chips, and it uses no bonding-specific equipment or materials. We emphasize that this method does not establish a galvanic connection between the chips, so care must be taken to avoid extraneous resonances if microwave frequencies are involved. The two chips communicate across the vacuum gap, for example with inductive or capacitive coupling, as described below.

Superconducting circuits are very sensitive to material loss[13–16], and the photoresist and photodefined-epoxy involved in this procedure could be problematic. We test this with a simple experiment where we bond superconducting coplanar waveguide resonators on one chip to a transmission line probe on the second chip, providing a good proxy for qubit measurements[17,18]. We use a standard "hanger" measurement configuration where we measure the transmission coefficient S_{21} through a transmission line that is coupled to a series of parallel coplanar waveguide resonators, but where the resonators and transmission line are on separate chips. In this experiment, resonators and transmission line are patterned on sapphire substrates, but this technique works with a wide

[a)] Present address: Google, Santa Barbara, California 93117, USA

[b)] Electronic mail: anc@uchicago.edu

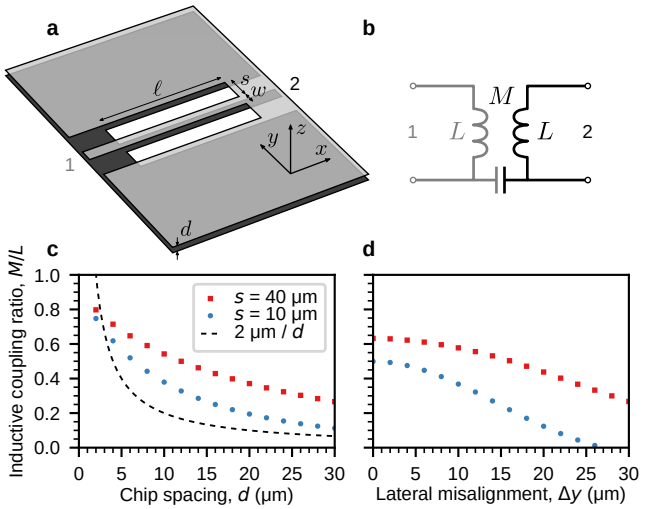

FIG. 1. **Inductive coupling scheme and simulations. a,** Schematic of two shorted coplanar waveguide segments, one on the surface of each chip. Each forms an inductor L, and they share a mutual inductance M due to their overlap of length ℓ. The coplanar waveguide has center trace width $w = 20\,\mu$m and center-to-ground plane conductor spacing $s = 40\,\mu$m; the two chips are separated by distance d. The two microwave ports are labeled 1 and 2. **b,** Circuit diagram for **a**. Note the capacitance between the ground planes of the two chips, which are not galvanically connected. **c,** Finite element simulation results for the inductive coupling ratio M/L as a function of inter-chip spacing d. We plot simulations for $s = 40\,\mu$m (as pictured in **a**) and $s = 10\,\mu$m, which gives a $\approx 50\,\Omega$ transmission line. We plot for comparison $(2\,\mu\text{m})/d$ to exhibit the $1/d$ dependence of a parallel plate capacitance; this falls off much more quickly with d than the mutual inductance. **d,** Additional simulation results, M/L versus lateral misalignment Δy, again for two values of s, with $d = 6.5\,\mu$m.

variety of materials. For example, in Ref. 7, a superconducting qubit patterned on sapphire is coupled using this technique to a surface acoustic wave resonator patterned on lithium niobate.

As there is no galvanic connection between the chips, they interact through free-space coupled electromagnetic fields. Two straightforward methods to engineer the coupling is via an inter-chip capacitance or a mutual inductance. Inductive coupling has a weaker dependence on the inter-chip vertical spacing d and can be established separately from the strong capacitive coupling between the (electrically separate) ground planes of the two chips. Inductive coupling is also compatible with superconducting coupling strategies involving tunable Josephson inductances.[7,19] In Fig. 1, we illustrate the method we use here, comprising inductive coupling between planar circuits on separate chips, achieved using short lengths of coplanar waveguide on each chip, aligned parallel to one another. Each coplanar waveguide is shorted to its respective ground plane, vertically separated by a distance d, as shown in Fig. 1a. Each coplanar waveguide segment acts as an inductor L, and in this arrangement, they share a mutual inductance M; the equivalent circuit is drawn in Fig. 1b.

We numerically simulate this geometry with finite element software (Sonnet Software, 126 N. Salina St., Syracuse NY 13202 USA), extracting the inductances L and M from the impedance matrix Z.[20] The ratio M/L, which can be at most unity, is a useful measure of the coupling we can achieve between the two chips. In Fig. 1c, we plot the simulated inductive coupling ratio M/L versus inter-chip distance d for this chosen geometry, with different ground-to-center strip spacings s. For comparison, we plot the $1/d$ dependence of a parallel-plate capacitor. The ratio M/L scales much more favorably with inter-chip distance d, decreasing by only about a factor of two as we change d from $2\,\mu$m to $20\,\mu$m. This weak distance dependence makes it easier to achieve strong and predictable interactions with larger ($\sim$10 μm) inter-chip distances, and makes the design robust to fabrication and assembly variations. We note that the ratio M/L does not reach unity because of the inductance of the non-overlapping portions of coplanar waveguide. In Fig. 1d, we show the effect of lateral misalignment Δy. The design is robust to lateral misalignment up to about $\Delta y \approx 10\,\mu$m, which is straightforward to achieve in the assembly process.

We employ the inductive coupling scheme to couple a quarter-wave coplanar waveguide resonator to a measurement coplanar waveguide on a separate chip. This is shown in the circuit diagram in Fig. 2a. This circuit is complementary to the usual capacitive "hanger" measurement.[14] Here, the measurement waveguide is under the short-circuit side of the quarter-wave resonator, where the current is maximized. The mutual inductance M allows energy to enter and leave the resonator through the measurement waveguide; this is quantified by the coupling quality factor

$$Q_c = \frac{1}{8\pi}\left(\frac{Z_0}{f_0 M}\right)^2, \tag{1}$$

where f_0 is the resonance frequency and $Z_0 \approx 50\,\Omega$ is the characteristic impedance of the coplanar waveguide. Following a calculation analogous to Ref. 14, we determine the normalized microwave transmission $\tilde{S}_{21}$ through the measurement waveguide, given by

$$\frac{1}{\tilde{S}_{21}} \approx 1 + e^{i\phi}\frac{Q_i}{Q_c}\frac{1}{1 + i2Q_i\delta x}, \tag{2}$$

where Q_i is the internal quality factor of the resonator, $\delta x = (f - f_0)/f_0$ is the relative frequency shift from resonance, and $e^{i\phi}$ is a phase factor accounting for a small series impedance mismatch $\Delta Z \ll Z_0$.

The inductive coupling geometry described in Fig. 1 can be varied quite a bit, with a feasible range of about two orders of magnitude in M, which equates to four orders of magnitude in the coupling strength Q_c. We design an experiment to test this by building eight coplanar waveguide resonators, each with a slightly different

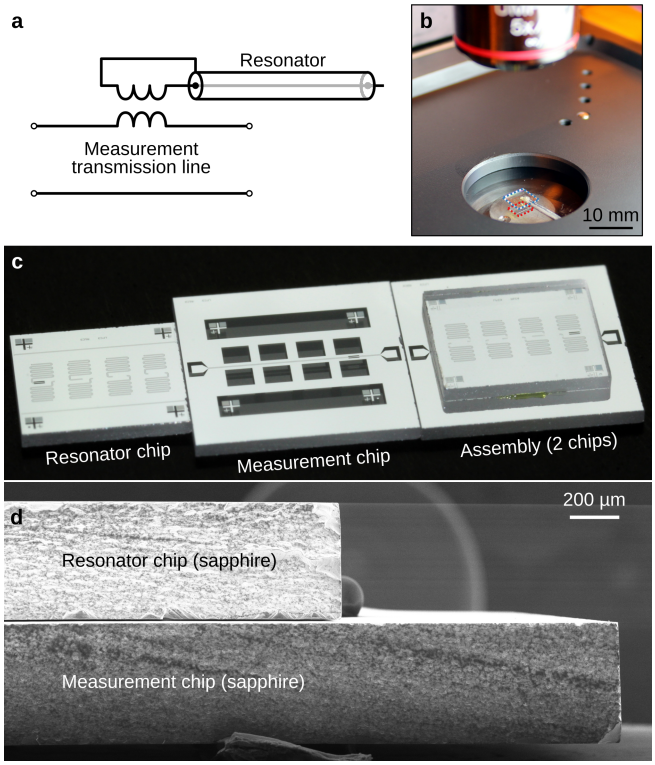

FIG. 2. **Flip-chip assembly. a,** Circuit diagram for a coplanar waveguide resonator inductively coupled to a measurement coplanar waveguide on a separate chip. The shorted end of the quarter-wave resonator is placed above the measurement transmission line, creating a mutual inductance between the transmission line and resonator. **b,** Photograph of the contact aligner during the assembly process. The two chips are outlined in blue (6 mm measurement chip) and red (4 mm resonator chip with epoxy spacers and glue). **c,** Photograph showing the flip-chip assembly. Right: Complete flip-chip assembly, which is made of a 4 mm chip with resonators inverted and attached to a 6 mm chip with a measurement transmission line. A small amount of glue is visible along the lower edge of the 4 mm chip. Center: A separate 6 mm chip with a measurement transmission line. Left: A separate 4 mm chip with resonators and epoxy spacers. **d,** Scanning electron micrograph of assembled chips, with an estimated spacing of 7 µm. A small amount of photoresist can be seen on the right side, at the join between the two chips.

length (hence resonance frequency), and each designed to have a different Q_c. The various coupler designs are listed in Table I. The mutual inductance is proportional to the coupler length ℓ_c. For resonator 1, we minimize Q_c (increasing the coupling) by using wider ground plane spacing $s_c = 40\,\mu\text{m}$ in the coupler, while for resonators 2 to 4, we gradually increase Q_c by decreasing the coupler length ℓ_c, and for resonators 5 to 8, we further increase Q_c by introducing an intentional lateral misalignment Δy between the coupler and the measurement waveguide.

The flip-chip assembly process is illustrated in Fig. 2b-d. We use standard techniques to evaporate a 100 nm

	s_c (µm)	ℓ_c (µm)	Δy (µm)	$f_{0,\text{Design}}$ (GHz)	$Q_{c,\text{Design}}$
1	40	300	0	5.25	2.3×10^2
2	10	300	0	5.37	6.9×10^2
3	10	100	0	5.49	6.0×10^3
4	10	40	0	5.93	3.2×10^4
5	10	40	5	5.85	4.5×10^4
6	10	40	10	5.76	6.3×10^4
7	10	40	15	5.67	1.5×10^5
8	10	40	20	5.59	5.9×10^5

TABLE I. Coupler designs for the eight coplanar waveguide resonators. The ground-center conductor spacing is s_c and the coupler length ℓ_c; Δy refers to the intentional lateral misalignment (see Fig. 1). The measured resonance frequencies f_0 are within 10% of the design frequencies, and the frequency spacings are as designed for resonances 3-8 (the two lowest-Q_c resonators were offset differently, perhaps due to their longer couplers). Outside the coupler region, the resonators and measurement transmission line are all coplanar waveguides with $w = 20\,\mu\text{m}$ and $s = 10\,\mu\text{m}$, giving $Z_0 \approx 50\,\Omega$. The coupling quality factors Q_c are based on the simulations in Fig. 1, with inter-chip distance $d = 6.5\,\mu\text{m}$.

film of aluminum on a clean double-side polished sapphire wafer and pattern the aluminum with photolithography followed by inductively-coupled plasma etching ($Cl_2/BCl_3/Ar$). We then pattern epoxy spacers (SU-8 3005 photoresist, 7 µm thick) prior to dicing the wafer. The epoxy spacers are only needed on one of the chips, and once the epoxy is hard-baked, it is resistant to solvents like acetone.

We bond the two chips together in a standard manual mask aligner (Karl Suss MJB4), shown in Fig. 2b. We use the mask vacuum to suspend one chip upside down, transferring the vacuum through a machined acrylic plate. This chip remains fixed in place, and it is important that it is double-side polished and transparent for alignment. The second chip has the resonators and epoxy spacers. The epoxy pattern is designed to contain the photoresist "glue" and prevent it from spreading to the resonators. We use nLOF 2070 photoresist as glue; it has a suitable viscosity for manual application, fills the gap between the chips well, and dissolves easily in acetone. We did observe that after two thermal cycles to cryogenic temperatures, the photoresist becomes quite brittle. We apply the photoresist manually using a splintered wooden dowel, using about 10 nL, covering roughly 2 mm along the two opposite edges of the chip. In the mask aligner, we align the chips and then bring them into contact. We then solidify the photoresist by heating the acrylic plate with a hot air gun (Aoyue 852, air 100 °C, chips ≈60 °C, for about 10 minutes). A photograph of a completed assembly is shown in Fig. 2c, and in Fig. 2d, we show a scanning electron micrograph of the assembly, viewed at near grazing incidence. The two chips are separated by about 7 µm, with a typical tilt of about 0.03°. Typical lateral alignment error is less than 2 µm in translation and 0.03° in rotation, measured with

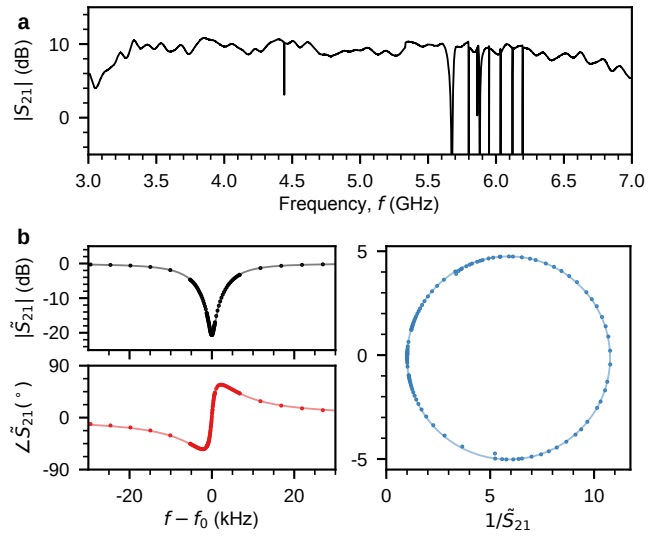

FIG. 3. **Microwave transmission measurements. a,** Raw transmission magnitude $|S_{21}|$ through the measurement transmission line. The overall level is arbitrary, dictated by attenuation and amplification in the signal path. There are eight coplanar waveguide resonances (5.6 GHz to 6.2 GHz) and an additional unidentified resonance at 4.5 GHz. This spurious resonance has $Q_i \approx 6 \times 10^4$ (much lower than the coplanar waveguide resonances) and $Q_c \approx 5 \times 10^4$. The frequency spacing of this scan is 31.25 kHz. **b,** Normalized transmission $\tilde{S}_{21}$ close to the highest-Q_c coplanar waveguide resonance. The magnitude $|\tilde{S}_{21}|$ (black) and phase $\angle\tilde{S}_{21}$ (red) are plotted versus frequency detuning $f - f_0$, where the resonator frequency is $f_0 = 5.862$ GHz. The inverse $1/\tilde{S}_{21}$ (blue) is plotted in the complex plane (horizontal axis: real part, vertical axis: imaginary part). This measurement is at relatively high power, with $n = 4.0 \times 10^6$ photons in the resonator. Solid lines are fits to Eq. 2.

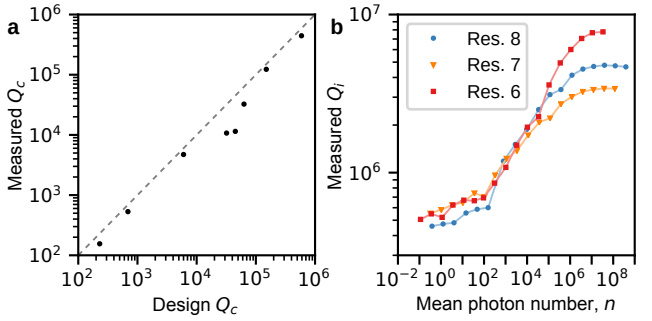

FIG. 4. **Quality factor measurements. a,** Measured coupling quality factor Q_c versus the design value. The dashed line represents the ideal case. Uncertainty in each fitted Q_c value is about 2%. **b,** Measured internal quality factor Q_i versus the mean photon number n for the three highest-Q_c resonances. Uncertainty in each fitted Q_i value is about 10%. Lines connect the measured data points.

vernier alignment marks included in the lithographic patterning. This is well within the tolerances suggested by the simulations in Fig. 1.

We characterize the device by cooling it in a dilution refrigerator (base temperature 7 mK) and measuring microwave transmission S_{21} through the device with a vector network analyzer (Agilent PNA-L). The device is wirebonded in an aluminum sample box with multi-stage magnetic shielding, the input line is heavily attenuated and filtered, and the output line includes a high electron mobility transistor amplifier at 4 K (Low Noise Factory) as well as room temperature amplifiers (Miteq AFS3). We show representative measurements in Fig. 3. In Fig. 3a, we measure transmission over a broad frequency range. The eight desired coplanar waveguide resonances are observed, ranging from 5.6 GHz to 6.2 GHz. There is an additional unidentified resonance near 4.5 GHz; it may be a slotline mode in the transmission line, a parallel plate mode between the chips, or a circulating mode around the perimeter of the floating chip. We reiterate that there is no galvanic connection between the two chips, which could support stray modes of this kind. In Fig. 3b, we show the detailed response for one resonance, the one with the highest Q_c. The magnitude is normalized to approach 0 dB off-resonance, and we subtract a linear offset from the phase. Following Ref. 14, we fit Eq. 2 to the measurement, from which we extract f_0, Q_i, Q_c, and the mean photon number n, which is proportional to the measurement power. We use similar measurements on the other resonances to determine their resonance frequencies, coupling quality factors Q_c (which are power-independent) and internal quality factors Q_i (which depend on power).

In Fig. 4, we summarize the fit quality factors. Fig. 4a compares the measured coupling quality factors Q_c to their design values, discussed above. We achieve the desired range of more than three orders of magnitude in Q_c, illustrating this technique's flexibility. The measured Q_c values are systematically lower than the design values; the simulations were two-port simulations as in Fig. 1, and more comprehensive simulation geometries may yield better results. Significantly, the effects of coupler spacing s_c, length ℓ_c, and lateral offset Δy are all consistent with the simulations. Fig 4b shows the measured internal quality factor Q_i versus the mean photon number n, which is proportional to the drive power. We perform power-dependent measurements on the three highest-Q_c resonances, as the measurement time is much faster when $Q_c \sim Q_i$. We observe the characteristic sigmoidal behavior, where Q_i decreases with n, reaching a plateau at the small $n \sim 1$ limit, with $Q_i \approx 5 \times 10^5$. This is about an order of magnitude lower than the high power ($n > 10^6$) measurements, and is consistent similar single-chip resonator measurements.[14]

In conclusion, we have demonstrated a simple method for flip-chip integration using only basic photolithography equipment. The inductive coupling scheme we use here is robust to errors in inter-chip distance and alignment, and it allows designs with a wide range of coupling

strengths. This technique is compatible with low-loss superconducting circuits, opening up a wide range of experiments integrating hybrid quantum systems, as devices with incompatible materials can be fabricated separately before being assembled together. A specific example is described in Ref. 7.

Acknowledgements

We thank P. J. Duda for helpful discussions. Devices and experiments were supported by the Air Force Office of Scientific Research and the Army Research Laboratory, and material for this work was supported by the Department of Energy (DOE). K.J.S. and S.J.W. were supported by NSF GRFP (NSF DGE-1144085), É.D. was supported by LDRD funds from Argonne National Laboratory, A.N.C. and D.D.A. were supported by the DOE, Office of Basic Energy Sciences, and D.I.S. acknowledges support from the David and Lucile Packard Foundation. This work was partially supported by the UChicago MRSEC (NSF DMR-1420709) and made use of the Pritzker Nanofabrication Facility, which receives support from SHyNE, a node of the National Science Foundation's National Nanotechnology Coordinated Infrastructure (NSF NNCI-1542205).

[1] A. D. O'Connell, M. Hofheinz, M. Ansmann, R. C. Bialczak, M. Lenander, E. Lucero, M. Neeley, D. Sank, H. Wang, M. Weides, J. Wenner, J. M. Martinis, and A. N. Cleland, Nature **464**, 697 (2010).

[2] K. Stannigel, P. Rabl, A. S. Sørensen, P. Zoller, and M. D. Lukin, Physical Review Letters **105** (2010), 10.1103/physrevlett.105.220501.

[3] I. Yeo, P.-L. de Assis, A. Gloppe, E. Dupont-Ferrier, P. Verlot, N. S. Malik, E. Dupuy, J. Claudon, J.-M. Gérard, A. Auffèves, G. Nogues, S. Seidelin, J.-P. Poizat, O. Arcizet, and M. Richard, Nature Nanotechnology **9**, 106 (2013).

[4] M. Schuetz, E. Kessler, G. Giedke, L. Vandersypen, M. Lukin, and J. Cirac, Physical Review X **5** (2015), 10.1103/physrevx.5.031031.

[5] G. Kurizki, P. Bertet, Y. Kubo, K. Mølmer, D. Petrosyan, P. Rabl, and J. Schmiedmayer, Proceedings of the National Academy of Sciences **112**, 3866 (2015).

[6] Y. Chu, P. Kharel, W. H. Renninger, L. D. Burkhart, L. Frunzio, P. T. Rakich, and R. J. Schoelkopf, Science **358**, 199 (2017).

[7] K. J. Satzinger, Y. P. Zhong, H.-S. Chang, G. A. Peairs, A. Bienfait, M.-H. Chou, A. Y. Cleland, C. R. Conner, É. Dumur, J. Grebel, I. Gutierrez, B. H. November, R. G. Povey, S. J. Whiteley, D. D. Awschalom, D. I. Schuster, and A. N. Cleland, Nature **563**, 661 (2018).

[8] Y. Chu, P. Kharel, T. Yoon, L. Frunzio, P. T. Rakich, and R. J. Schoelkopf, Nature **563**, 666 (2018).

[9] M. Pltner, G. Sadowski, S. Rzepka, and G. Blasek, Microelectronics International **8**, 27 (1991).

[10] J. H. Lau, ed., *Flip Chip Technologies* (McGraw-Hill, 1996).

[11] D. Rosenberg, D. Kim, R. Das, D. Yost, S. Gustavsson, D. Hover, P. Krantz, A. Melville, L. Racz, G. O. Samach, S. J. Weber, F. Yan, J. L. Yoder, A. J. Kerman, and W. D. Oliver, npj Quantum Information **3** (2017), 10.1038/s41534-017-0044-0.

[12] B. Foxen, J. Y. Mutus, E. Lucero, R. Graff, A. Megrant, Y. Chen, C. Quintana, B. Burkett, J. Kelly, E. Jeffrey, Y. Yang, A. Yu, K. Arya, R. Barends, Z. Chen, B. Chiaro, A. Dunsworth, A. Fowler, C. Gidney, M. Giustina, T. Huang, P. Klimov, M. Neeley, C. Neill, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. C. White, and J. M. Martinis, Quantum Science and Technology **3**, 014005 (2017).

[13] A. D. O'Connell, M. Ansmann, R. C. Bialczak, M. Hofheinz, N. Katz, E. Lucero, C. McKenney, M. Neeley, H. Wang, E. M. Weig, A. N. Cleland, and J. M. Martinis, Applied Physics Letters **92**, 112903 (2008).

[14] A. Megrant, C. Neill, R. Barends, B. Chiaro, Y. Chen, L. Feigl, J. Kelly, E. Lucero, M. Mariantoni, P. J. J. O'Malley, D. Sank, A. Vainsencher, J. Wenner, T. C. White, Y. Yin, J. Zhao, C. J. Palmstrøm, J. M. Martinis, and A. N. Cleland, Applied Physics Letters **100**, 113510 (2012).

[15] C. M. Quintana, A. Megrant, Z. Chen, A. Dunsworth, B. Chiaro, R. Barends, B. Campbell, Y. Chen, I.-C. Hoi, E. Jeffrey, J. Kelly, J. Y. Mutus, P. J. J. O'Malley, C. Neill, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. C. White, A. N. Cleland, and J. M. Martinis, Applied Physics Letters **105**, 062601 (2014).

[16] C. Wang, C. Axline, Y. Y. Gao, T. Brecht, Y. Chu, L. Frunzio, M. H. Devoret, and R. J. Schoelkopf, Applied Physics Letters **107**, 162601 (2015).

[17] H. Wang, M. Hofheinz, J. Wenner, M. Ansmann, R. C. Bialczak, M. Lenander, E. Lucero, M. Neeley, A. D. O'Connell, D. Sank, M. Weides, A. N. Cleland, and J. M. Martinis, Applied Physics Letters **95**, 233508 (2009).

[18] A. Dunsworth, A. Megrant, C. Quintana, Z. Chen, R. Barends, B. Burkett, B. Foxen, Y. Chen, B. Chiaro, A. Fowler, R. Graff, E. Jeffrey, J. Kelly, E. Lucero, J. Y. Mutus, M. Neeley, C. Neill, P. Roushan, D. Sank, A. Vainsencher, J. Wenner, T. C. White, and J. M. Martinis, Applied Physics Letters **111**, 022601 (2017).

[19] Y. Chen, C. Neill, P. Roushan, N. Leung, M. Fang, R. Barends, J. Kelly, B. Campbell, Z. Chen, B. Chiaro, A. Dunsworth, E. Jeffrey, A. Megrant, J. Y. Mutus, P. J. J. O'Malley, C. M. Quintana, D. Sank, A. Vainsencher, J. Wenner, T. C. White, M. R. Geller, A. N. Cleland, and J. M. Martinis, Physical Review Letters **113** (2014), 10.1103/physrevlett.113.220502.

[20] D. M. Pozar, *Microwave Engineering* (Wiley, 2012).